

Günhan Dündar

**Department of Electrical and Electronic Engineering
Boğaziçi University
Bebek 80815, İstanbul
Turkey**

**Tel: (212) 358 1540 / ext. 1860
Fax: (212) 287 2465
e-mail: dundar@boun.edu.tr**

Education

- [1993] Ph.D., Electrical, Computer, and Systems Engineering
Rensselaer Polytechnic Institute, USA
Thesis: CMOS VLSI Design of Analog Neural Networks.
- [1991] M.S., Electrical and Electronic Engineering
Boğaziçi University, Turkey.
Thesis: A Comparative Evaluation of Edge Detectors and Preprocessing Algorithms.
- [1989] B.S., Electrical and Electronic Engineering
Boğaziçi University, Turkey.

Awards

- The Vehbi Koç foundation award for the first 20 in the university entrance exam (1985-1989)
- Boğaziçi University Research Fund Award (1996)
- Boğaziçi University Foundation Encouragement Award (2000, 2001,2002,2003)
- Boğaziçi University Foundation Young Researcher Award (2002)

Experience

- 5/2002 – present: Full Professor, Boğaziçi University
- 9/2002 – 6/2003: Invited Professor, EPFL.

- 4/97 – 5/2002: Associate Professor, Boğaziçi University. Taught VLSI Design, Advanced VLSI Design, Computational VLSI, Electronic Circuits I and II, Electronics Laboratory, and Neural Networks.
- 6/96 – 4/97: Assistant Professor, Boğaziçi University. Taught a graduate course in computational VLSI and a second course in electronic circuits for junior level students.
- 1/94 – 6/96: Instructor, Boğaziçi University, Department of Electrical and Electronic Engineering. Taught graduate courses on microelectronic design, computational aspects of VLSI design, and semiconductor device theory. Taught undergraduate courses on introductory electronics for both electrical engineering and computer engineering students. Conducted electronic circuit labs.
- 11/94 – 12/95: Instructor, Naval Academy, taught Electronics Lab 1, Signals and Systems, Electronics Lab 2, and Digital Electronics.
- 8/94 – 12/95: Military service with the Turkish Navy.
- 1/94 – 6/94: Instructor, Air Force Academy, taught a course in Computer Networks.
- 7/90 – 7/91: Teaching Assistant, Boğaziçi University, Turkey. Held counseling hours for 5 junior/senior level courses on electronic circuits, digital electronic circuits and communication circuits. Instructed three electronics lab classes.
- 12/87 – 1/88: Trainee Engineer, Ekacomp, İstanbul. Worked in the servicing of microcomputers.
- 8/87 – 8/87: Trainee Engineer, Grundig, İstanbul.
- 6/87 – 8/87: Trainee Engineer, Philips, İstanbul. Worked in designing test benches for TV sets.

Areas of Research Interest

- Analog IC design
- Architectural modeling and circuit design of DSP and image processing systems.
- Design of analog neural networks
- Electronic design automation
- Image processing and data compression algorithms

Research Projects Conducted to Completion

- A Design automation and modeling system for A/D Converters, *for TÜBİTAK (The Scientific and Technical Research Council of Turkey)*, Project No:101E039, 2001-2004
- Implementation of artificial neural networks with analog integrated circuits, *for TÜBİTAK (The Scientific and Technical Research Council of Turkey)*, Project No:EEEAG-183, 1996-1998.
- ALG: An Analog Layout Generator, *for Boğaziçi University Research Fund*, 1996-1999.

Technical Training

- NATO ASI on Computational Intelligence, Turkey, August 1996.
- NATO ASI on System Level Synthesis, Italy, August 1998.
- RF Circuit Design for Wireless Communications, Switzerland, July 2000.

Administrative and Academic Services

- Member of the Curriculum, Faculty Search, PhD administration, and Technical Support Committees, Department of Electrical and Electronic Engineering, Boğaziçi University, 1998-present.
- Member of KOSGEB (Small Scale Industry Development Support) Evaluation Committee, Boğaziçi University, 1998-present.
- Member of BİM (Computing Facilities) Committee (1998-2004), Boğaziçi University.
- Member of Boğaziçi University Press Committee (2004-present).
- Vice Chairman of the Electrical and Electronic Engineering Department, Boğaziçi University, 2003-2006
- Chairman of the Electrical and Electronic Engineering Department, Boğaziçi University, 2006-present

Conferences Organized

- Turkish Artificial Intelligence and Neural Networks Symposium, June 1999.

Seminars and Invited Talks

- G. Dündar: “ANNSyS – An Analog Neural Network Synthesis System”, University of Genoa, Genoa, Italy, August 1998.
- G. Dündar: “Non-idealities and component variations in analog neural networks”, Georgia Institute of Technology, Atlanta, Georgia, USA, August 1999.
- G. Dündar: “Design automation of analog integrated circuits”, EPFL, Lausanne, Switzerland, October 2002.

Courses to the Industry

- S. Balkır and G. Dündar: “Design Automation of Digital Circuits Using Mentor Graphics Software”, Havelan, İstanbul, 1996.

M.S. Theses Conducted to Completion

- Top-down Design of CMOS Based Subsystems for DSP.
Student: Hakan Binici, Co-advisor: Sina Balkır, Date: 1995.
- Circuit Simulation Based Training Algorithms for Analog Neural Networks.
Student: İsmet Bayraktaroğlu, Co-advisor: Sina Balkır, Date: 1996.
- VLSI Implementation of a Neural Network Based Fuzzy Logic Controller.
Student: Mustafa Sözer, Date: 1998.
- VLSI Implementation of a New Standard for Lossless Compression of Continuous Tone Still Images.
Student: A. Suat Aktürk, Co-advisor: Sina Balkır, Date: 1998.
- Analog VLSI Implementation of Wavelet Transforms Using Switched Capacitor Filters.
Student: Gürkan Sönmez, Co-advisor: Sina Balkır, Date: 1997.
- Amendment of Firing Mechanisms of Destructors Based on Development of Software and All Digital Circuitry.
Student: İhsan Bakar, Co-advisor: Ömer Cerid, Date: 1997.
- Amendment of Firing Mechanisms of Destructors Based on Development of Hardware Solid State Sensors and All Analog Interfacing Circuitry.
Student: Ayhan Bay, Co-advisor: Ömer Cerid, Date: 1997.
- ALG: An Analog Layout Generator.
Student: Altuğ Şimşek, Co-advisor: Sina Balkır, Date: 1997.
- A Fast and Accurate Delay Estimation Method for Adders as CMOS Arithmetic Building Blocks in VLSI Design.
Student: Gökhan Karakuş, Co-advisor: Sina Balkır, Date: 1998.
- An Optimized Method for the Estimation of Power Dissipation in Adders as CMOS Arithmetic Building Blocks.
Student: Arsal Dikel, Co-advisor: Sina Balkır, Date: 1998.
- Design of a High Resolution ADC.
Student: Serhan Eröz, Co-advisor: Sina Balkır, Date: 1998.
- VLSI Implementation of a Secure Communication System Using Current-Mode Chaotic Circuits
Student: Sedat Nişancı, Co-advisor: Sina Balkır, Date: 1999.
- Design of a Microcontroller Board and Development of Software for Ultrasonic Radar
Student: Nilüfen Çotuk, Co-advisor: Ömer Cerid, Date: 1999.
- Hardware Implementation of Ultrasonic Radar System and Microcontroller Interfacing
Student: Levent Bektaş, Co-advisor: Ömer Cerid, Date: 1999.
- Feedforward Neural Network Optimization Suitable for Hardware Implementation
Student: Devrim Albuz, Date: 1999.
- Traffic Modeling in ATM Switches Using Neurofuzzy Methods
Student: Amer Çatoviç, Co-advisor: Sema Oktuğ, Date: 1998.
- High-Level Synthesis of Analog Circuits
Student: İ. Gökhan Erten, Co-advisor: Sina Balkır, Date: 1999.
- Performance Comparison of Viterbi Decoders

Student: Levent Çetrez, Date: 2000.

- Performance Estimation in Analog CAD
Student: İ. Faik Başkaya, Date: 2000.
- Theoretical Prediction of Parameter Quantization Effects in Gaussian Potential Function Neural Networks
Student: Erkan Karakuş, Date: 2000.
- Architectures and Implementations for Speech Enhancement
Student: Gökhan Coşğul, Date: 2000.
- Weight Quantization for Multilayer Perceptrons
Student: Fatih Köksal, Co-advisor: Ethem Alpaydın, Date: 2000.
- Logic Level Power Estimation in CMOS VLSI Circuits
Student: Mustafa Aktan, Date: 2001.
- High Level Modeling and Optimization of A/D Converters
Student: Selçuk Talay, Date: 2001.
- Design and Implementation of 3.2 Gbps LVDS Receiver
Student: Erdem Karaadam, Date: 2002.
- An Optimization-based Hierarchical Design Automation System
Student: Öszun Serkan Sönmez, Date: 2003.
- An Analog Performance Estimation System Based on BSIM Models
Student: Balkır Kayaaltı, Date: 2003.
- A Layout advisor for Analog Layouts
Student: Mehmet Selçuk Ataç, Date: 2003.
- A Single-chip solution for text-to-speech synthesis
Student: Ozan Aktan, Date: 2004.
- Development of a library for CMOS analog neural networks
Student: Mustafa Taşkaldıran, Date: 2004.
- Analog Design automation System “Performance Estimation”
Student: Engin Deniz, Date: 2004.
- A Study of phase noise in differential CMOS LC Voltage Controlled Oscillators
Student: Oktay Güryay, Date: 2004.
- An Analytical modeling approach to the design of PLL’s
Student: Şeref Ersin Ak, Date: 2004.
- Analog Layout Generation
Student: Ender Yılmaz, Date: 2006.
- Analog Design and Optimization of PWL circuits used in fuzzy logic solutions
Student: Yankı Yalçın, Date: 2006.
- Power Analysis and Low Power Realization of Digital Filter Structures.
Student: Okan Zafer Batur, Date: 2006.

PhD Theses Conducted to Completion

- A Silicon Compiler for Multirate DSP Systems
Student: Arda Yurdakul, Co-advisor: Sabih Tansal, Date: 1999.
- Multilayer Perceptron Neural Networks in Analog VLSI – A System Level Study
Student: A. Selçuk Öğrenci, Co-advisor: Sina Balkır, Date: 1999.
- A New Approach to Analog Integrated Circuit Optimization
Student: Güner Alpaydın, Co-advisor: Sina Balkır, Date: 2000.
- Analysis and Modeling of Multi-gate MOSFET Structures
Student: Koray Karahaliloğlu, Date: 2002.

Personal Information

Birth Place and Date: Istanbul, 1969

Marital Status: Married

Children: One

Foreign Languages: English (fluent), German (medium), Italian (beginner), French (beginner).

Nationality: Turkish

Journal Publications

1. K. Karahaliloğlu and G. Dündar, "An explicit current model for dual gate MOSFET," *Solid State Electronics*, Vol. 47, No. 11, pp. 2117-2125, 2003.
2. G. Alpaydın, S. Balkır, and G. Dündar, "An evolutionary approach to automatic synthesis of high performance analog integrated circuits," *IEEE Transactions on Evolutionary Computing*, Vol. 7, No. 3, pp. 240-257, 2003.
3. S. Minaei, O. Cicekoglu, H. Kuntman, G. Dündar, and O. Cerid, "New realizations of current-mode and voltage-mode multifunction filters without external passive elements," *AEU-International Journal Of Electronics And Communications*, Vol. 57, No. 1, pp. 63-69, January 2003.
4. A. Yurdakul and G. Dündar, "Fast and efficient algorithm for the multiplierless realization of linear DSP transforms," *IEE Proceedings – Circuits, Devices, and Systems*, Vol. 149, No. 4, pp. 205-211, August 2002.
5. G. Alpaydın, G. Dündar, and S. Balkır, "Evolution based design of neural fuzzy networks using self-adapting genetic parameters," *IEEE Transactions on Fuzzy Systems*, Vol. 10, No. 2, pp. 211-221, April 2002.
6. A. Chatovich, S. Oktuğ, and G. Dündar, "Hierarchical neuro-fuzzy call admission controller for ATM networks," *Computer Communications*, Vol. 24, No. 11, pp. 1031-1044, June 2001.
7. A. S. Öğrenci, G. Dündar, and S. Balkır, "Fault tolerant training of neural networks in the presence of MOS transistor mismatches," *IEEE Transactions on Circuits and Systems*, Vol. 48, No.3, pp. 272-281, March 2001.
8. G. Alpaydın, G. Erten, S. Balkır, and G. Dündar, "Multi-level optimization approach to switched capacitor filter synthesis," *IEE Proceedings – Circuits, Devices, and Systems*, Vol. 147, No. 4, pp. 243-250, August 2000.
9. B. E. Sağlam, G. Coşgöl, and G. Dündar, "Comments on a systematic approach for design of digit-serial signal processing architectures," *IEEE Transactions on Circuits and Systems -II*, Vol. 47, No. 4, pp. 369 - 370, April 2000.
10. E. Yazıcıoğlu, S. Balkır, G. Dündar, and H. Çağlar, "Implementation of a new orthogonal shuffled block transform for image coding applications," *Journal of Real Time Imaging*, Vol. 6, No. 1, pp. 39 – 46, February 2000.
11. A. Yurdakul and G. Dündar, "Multiplierless realization of linear DSP transforms by using common two-term expressions," *Journal of VLSI Signal Processing*, Vol. 22, No. 3, pp. 163 – 172, September 1999.
12. A. Yurdakul and G. Dündar, "Statistical methods for the estimation of quantization effects and determination of optimal quantization stepsize in FIR-based multirate systems," *IEEE Transactions on Signal Processing*, Vol. 47, No. 6, pp. 1749-1753, June 1999.
13. İ. Bayraktaroğlu, A.S. Öğrenci, G. Dündar, S. Balkır, and E. Alpaydın, "ANNSyS: An Analogue Neural Network Synthesis System," *Neural Networks*, Vol. 12, No. 2, pp. 325-338, March 1999.
14. A. Şimşek and G. Dündar, "An application of self organizing neural networks to circuit partitioning," *ELEKTRİK, Turkish Journal of Electrical Engineering and Computer Sciences*, Vol. 4, Supplement, pp. 10 - 21, 1996.
15. G. Dündar, F-C. Hsu, and K. Rose, "Effects of nonlinear synapses on multilayer neural networks," *Neural Computation*, Vol. 8, No. 5, pp. 939-949, July 1996.
16. G. Dündar and K. Rose, "Comparing models for the growth of silicon-rich-oxides (SRO)," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 9, No. 1, pp. 74-81, Feb. 1996.

17. G. Dündar and K. Rose, "The effects of quantization on multilayer neural networks," *IEEE Transactions on Neural Networks*, Vol. 6, No. 11, pp. 1446 - 1451, Nov. 1995.
18. Ö. Cerid, S. Balkır, and G. Dündar, "Novel CMOS reference current generator," *International Journal of Electronics*, Vol. 78, No. 6, pp. 1113-1118, June 1995.
19. Ö. Cerid, S. Balkır, and G. Dündar, "Design automation of digital integrated circuits," *Hava Harp Okulu Bülteni*, Vol. 13, No. 36, pp. 29-37, July 1994 (in Turkish).
20. Ö. Cerid, S. Balkır, and G. Dündar, "Structural modeling and simulation of pipelined radix-2ⁿ multipliers," *Hava Harp Okulu Bülteni*, Vol. 13, No. 35, pp. 49-55, April 1994 (in Turkish).

Conference Publications

1. Y.D. Gökdel, S. Talay, G. Dündar and A. Meriç, "High Performance Sigma-Delta ADC with adaptive gain controller" Proceedings of ELECO'06, 6-10 December 2006, Bursa, Turkey.
2. S. Talay, E. Deniz, and G. Dündar, "A Sigma-Delta ADC design automation tool with embedded performance estimator," *Proceedings of MIXDES'06*, pp. 142-146, June 22-24 2006, Gdynia, Poland.
3. E. Yılmaz and G. Dündar, "A New performance oriented module generator," *Proceedings of MIXDES'06*, pp. 202-206, June 22-24 2006, Gdynia, Poland.
4. B. Koç, A. Koukab, and G. Dündar, "Phase noise in bipolar and CMOS VCO's – an analytical comparison," *Proceedings of ISCAS'06*, pp. 5688-5691, May 21-24 2006, KOS, Greece.
5. B.M. Wilamowski, M.E. Sinangil, and G. Dündar, "A Gray-Code current Mode ADC structure," *Proceedings of IEEE MELECON*, May 16-19 2006, Benalmadena, Spain.
6. O. Aktan, İ.F. Başkaya, and G. Dündar, "A single chip solution for text-to-speech synthesis," *Proceedings of ECCTD'05*, August 29-September 2, 2005, Cork City, Ireland.
7. E. Deniz and G. Dündar, "MOSFET modeling with EKV 2.6 and analog circuit design strategy for performance estimation tool," *Proceedings of ELECO'05*, pp. 28-32, 7-11 December 2005, Bursa, Turkey.
8. Ö. Gürsoy, O. Sağlamdemir, M. Aktan, S. Talay, and G. Dündar, "Low power decimation filter architectures for sigma-delta ADC's," *Proceedings of ELECO'05*, pp. 72--75, 7-11 December 2005, Bursa, Turkey.
9. E. Deniz and G. Dündar, "Performance estimator for an analog design automation system using EKV modeled analog circuits," *Proceedings of ECCTD'05*, August 29-September 2, 2005, Cork City, Ireland.
10. K. Atasü, G. Dündar, and C. Özturan, "An integer linear programming approach for identifying instruction set extensions," *Proceedings of CODES+ISSS'05*, Sept. 19-21, 2005, Jersey City, New Jersey.
11. M. Aktan and G. Dündar, "Design of digital filters for low power applications using integer quadratic programming," *Proceedings of PATMOS'05*, pp.137-145, Sept 21-23, 2005.
12. S. Talay and G. Dündar, "A Sigma-Delta ADC design automation tool," *Proceedings of PRIME 2005*, pp. 40-43, July 25-28 2005, Lausanne, Switzerland.
13. S. Talay and G. Dündar, "A Pipeline ADC Design with an ADC design automation system," *Proceedings of ELECO 2004*, pp. 140-144, Dec. 8-12, 2004, Bursa, Turkey (in Turkish).
14. M. Taşkaldıran and G. Dündar, "Development of a library for CMOS analog neural networks," *Proceedings of TAINN 2004*, pp. 361-368, June 10-11 2004, İzmir, Turkey.
15. S. Talay and G. Dündar, "Slew rate effects in first order sigma-delta ADC's," *Proceedings of MELECON 2004*, pp. 95-98, May 12-15 2004, Dubrovnik, Croatia.
16. İ.F. Başkaya, O. Aktan, and G. Dündar, "Text-to-speech integrated circuit," *Proceedings of SIU 2004*, pp.653-656, April 25-28 2004, Kuşadası, Turkey (in Turkish).
17. M. Aktan, U. Çini, and G. Dündar, "Design of digital filters for low-power applications by reducing the Hamming distance of the filter coefficients using mean field annealing algorithm," *Proceedings of SIU 2004*, pp.646-648, April 25-28 2004, Kuşadası, Turkey (in Turkish).

18. S. Talay and G. Dündar, "Jitter model of sigma-delta converters," *Proceedings of SIU 2004*, pp.371-374, April 25-28 2004, Kuşadası, Turkey (in Turkish).
19. S. Talay and G. Dündar, "High speed design tool for flash and pipeline ADC's," *Proceedings of ECCTD'03*, pp. II-213 – II-216, Sept 1-4 2003, Cracow, Poland.
20. S. Talay and G. Dündar, "Modeling of Sigma-Delta converters in MATLAB," *Proceedings of SIU 2003*, pp. 257-260, June 18-20, 2003, İstanbul, Turkey (in Turkish).
21. H. Sunar, G. Dündar, and E. Anarım, "IC Realization of multiwavelet filters," *Proceedings of SIU 2002*, pp. 1307 – 1312, June 12-14, 2002, Pamukkale, Turkey. (in Turkish)
22. G. Tulunay, G. Dündar, and A. Ataman, "A new approach to modeling statistical variations in MOS transistors," *Proceedings of ISCAS 2002*, pp. I-757 – I-760, May 26-29, 2002, Phoenix, Arizona.
23. G. Alpaydın, S. Balkır, and G. Dündar, "Evolution based automatic synthesis of analog integrated circuits," *Proceedings of ISCAS 2002*, pp. II-65 – II-68, May 26-29, 2002, Phoenix, Arizona.
24. K. Karahaliloğlu and G. Dündar, "Analytical current model for dual gate MOSFET," *Proceedings of ICECS'2001*, pp. 1015-1019, September 2-5, 2001, Malta.
25. İ. F. Başkaya and G. Dündar, "Performance estimation in analog computer aided design," *Proceedings of ECCTD'2001*, pp.II-117 – II-120, August 28-31, 2001, Espoo, Finland.
26. F. Köksal, E. Alpaydın, and G. Dündar, "Weight quantization for multilayer perceptrons using soft weight sharing," *Proceedings of ICANN'2001*, pp. 211-216, August 21-25, 2001, Vienna, Austria.
27. E. Karakuş, A. S. Öğrenci, and G. Dündar, "Parameter quantization effects in Gaussian potential function neural networks," *Advances in Neural Networks and Applications*, pp. 247 – 252, February 11 – 15, 2001, Puerto de la Cruz, Spain.
28. D. Albuz, A.S. Öğrenci, and G. Dündar, "Using sensitivity analysis for weight quantization," *Proceedings of TAINN'2000*, pp. 127 – 136, June 21 - 23, 2000, İzmir, Turkey.
29. F. Köksal, E. Alpaydın, and G. Dündar, "Weight quantization for multilayer perceptrons," *Proceedings of TAINN'2000*, pp. 137 – 146, June 21 – 23, 2000, İzmir, Turkey.
30. İ.C. Çevikbaş, A.S. Öğrenci, G. Dündar, and S. Balkır, "VLSI implementation of GRBF (Gaussian Radial Basis Function) networks," *Proceedings of ISCAS'00*, pp. III-646 – III-649, May 28 – 31, 2000, Geneva, Switzerland.
31. G. Alpaydın, G. Coşgöl, G. Dündar, and S. Balkır, "Fuzzy performance model of mismatch for analog integrated circuit optimization," *Proceedings of ECCTD'99*, pp. 1099-1102, Aug. 30 – Sept. 2, 1999, Stresa, Italy.
32. S. Nişancı, G. Dündar, S. Balkır, and Y. Denizhan, "IC design for secure communication using current-mode chaotic circuits," *Proceedings of ECCTD'99*, pp. 880-883, Aug. 30 – Sept. 2, 1999, Stresa, Italy.
33. G. Alpaydın, G. Erten, S. Balkır, and G. Dündar, "Synthesis of switched capacitor filters in a multi-level optimization environment," *Proceedings of the Third International Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, pp. 175 – 178, July 26-28, 1999, Puerto Vallarta, Mexico.
34. G. Erten, G. Dündar, and S. Balkır, "Optimization and synthesis of switched current filters with non-ideal MOS transistors," *Proceedings of the Third International Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, pp. 13 – 17, July 26-28, 1999, Puerto Vallarta, Mexico.
35. A. Çatoviç, S. Oktuğ, and G. Dündar, "Hierarchical neuro-fuzzy call admission controller for ATM networks," *Proceedings of IFIP'99*, June 28-30, Antwerp, Belgium.

36. G. Alpaydın, G. Dündar, and S. Balkır, "Optimization of neural fuzzy networks," *Proceedings of TAINN'99*, pp. 154 – 162, June 23-25, 1999, Istanbul, Turkey.
37. G. Coşğül, A. S. Öğrenci, and G. Dündar, "Neural network based CAD tool for modeling manufacturing variations in MOS devices," *Proceedings of TAINN'99*, pp. 202 – 209, June 23-25, 1999, Istanbul, Turkey.
38. A. S. Öğrenci, M. Becer, G. Dündar, and S. Balkır, "Incorporating MOS transistor mismatches into training of analog neural networks," *Proceedings of NC'98*, pp. 669 – 675, Sept. 1998, Vienna, Austria.
39. İ. F. Başkaya and G. Dündar, "Test pattern generation for VLSI neural networks," *Proceedings of TAINN'98*, pp. 43 - 52, June 24 - 26, 1998, Ankara, Turkey.
40. A. Yurdakul and G. Dündar, "Multiplierless realization of FIR-based multirate systems by using common two-term expressions," *Proceedings of SIU'98*, Vol. 2, pp. 525 - 530, May 28-30, 1998, Kızılcıhamam, Turkey. (in Turkish).
41. G. Hafız, G. Dündar, S. Balkır, and L. Akın, "Optimization of analog integrated circuits via simulated annealing and evolutionary strategies," *Proceedings of ECCTD'97*, pp. 502-506, Sept. 1-4, 1997, Budapest, Hungary.
42. İ. Bayraktaroğlu, A. S. Öğrenci, G. Dündar, S. Balkır, and E. Alpaydın, "ANNSyS: An Analog Neural Network Synthesis System," *Proceedings of ICNN'97*, Vol 2, pp. 910 - 915, June 9-13, 1997, Houston, Texas.
43. İ. G. Erten, A. S. Öğrenci, and G. Dündar, "A compaction algorithm for SAFANN," *Proceedings of TAINN'97 (New Trends in Artificial Intelligence and Neural Networks)*, pp. 227 - 231, May 22 -23, 1997, Kızılcıhamam, Turkey.
44. E. Yazıcıoğlu, G. Dündar, S. Balkır, and H. Çarlar, "VLSI Design of shuffled block transform and inverse transform architectures," *Proceedings of SIU'97*, Vol. 2, pp. 679 - 684, May 1-3, 1997, Kuşadası, Turkey. (in Turkish)
45. A. Yurdakul and G. Dündar, "The effects of finite wordlength on FIR filters and the reflection on multiresolution systems," *Proceedings of SIU'97*, Vol. 2, pp. 593 - 598, May 1-3, 1997, Kuşadası, Turkey. (in Turkish).
46. A. S. Öğrenci, G. Dündar, S. Balkır, and E. Alpaydın, "Training of multilayer neural networks with non-linear multipliers from analog integrated circuits," *Proceedings of SIU'97*, Vol. 2, pp. 656 - 660, May 1-3, 1997, Kuşadası, Turkey. (in Turkish).
47. İ. Bayraktaroğlu, A. S. Öğrenci, G. Dündar, and S. Balkır, "On-chip training by software for analog neural networks using ANNSyS," *Proceedings of the 6th NASA Symposium on VLSI Design*, pp. 3.3.1 - 3.3.10, March 5-6, 1997.
48. İ. Bayraktaroğlu, S. Balkır, and G. Dündar, "A circuit level simulator for analog neural networks," *Proceedings of the 5th Turkish Symposium on Artificial Intelligence and Neural Networks*, pp 305-310, June 27-28, 1996.
49. A. Şimşek and G. Dündar, "An application of self organizing neural networks to circuit partitioning," *Proceedings of the 5th Turkish Symposium on Artificial Intelligence and Neural Networks*, pp 91-100, June 27-28, 1996.
50. A. S. Öğrenci and G. Dündar, "SAFANN: Silicon Assembler for Analog Neural Networks," *Proceedings of the 5th Turkish Symposium on Artificial Intelligence and Neural Networks*, pp 311-316, June 27-28, 1996.
51. A. Yurdakul and G. Dündar, "A new hybrid algorithm for over the cell routing," *Proceedings of Melecon'96*, Vol. III, pp 480-483, May 13-16, 1996, Bari.
52. Ş. Özev, A. Altınordu, and G. Dündar, "Implementation of a radix-2n multiplier using high performance logic," *Proceedings of Melecon'96*, Vol. III, pp 469-472, May 13-16, 1996, Bari.

53. A. Şimşek, M. Civelek, and G. Dündar, "Study of the effects of nonidealities in multilayer analog neural networks with circuit level simulation," *Proceedings of Melecon'96*, Vol. I, pp 613-616, May 13-16, 1996, Bari.
54. Y. Atabek, G. Dündar, S. Balkır, H. Çağlar, and E. Anarım, "Design of M-band wavelet filter with perfect reconstruction architecture," *Proceedings of the International Conference on Telecommunications*, pp. 225-229, April 14-17, 1996.
55. G. Elbek, S. Balkır, and G. Dündar, "Design and simulation of a two band three level wavelet decomposition architecture using folding algorithm," *Proceedings of the International Conference on Telecommunications*, pp. 178-182, April 14-17, 1996.
56. Y. Atabek, G. Dündar, S. Balkır, H. Çağlar, and E. Anarım, "Design of M-band analysis and perfect reconstruction filters," *Proceedings of SIU'96*, Kemer, Türkiye, pp. 253-258, April 5-6, 1996 (in Turkish).
57. G. Elbek, S. Balkır, and G. Dündar, "Design and VLSI realization of a two band three level wavelet decomposition architecture," *Proceedings of SIU'96*, Kemer, Türkiye, pp. 325-330, April 5-6, 1996 (in Turkish).
58. H. Binici, G. Dündar, and S. Balkır, "A new multiplier based on radix-2 conversion scheme," *Proceedings of the European Conference on Circuit Theory and Design*, pp. 439-442, August 1995.
59. S. Gören, S. Balkır, G. Dündar, and E. Anarım, "Novel VLSI architectures for morphological filtering" *Proceedings of the IEEE Workshop on Morphological Signal Processing*, pp. 875-878, June 22, 1995.
60. S. Gören, S. Balkır, G. Dündar, and E. Anarım, "Novel VLSI architectures for morphological filtering," *Proceedings of SIU'95*, Nevşehir, Türkiye, Book A. Image Processing, pp. 187-192, April 26-28, 1995 (in Turkish).
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