EE Department Seminars December 23, 2013, Monday, 15:00

Yorgo Istefanopulos Meeting Lounge

QUALITY AND RELIABILITY OF ANALOG AND MIXED-SIGNAL CIRCUITS: MODELING, SIMULATION, TESTING

Mustafa Berke Yelten, PhD
Intel Corporation, Hillsboro, OR, USA

Quality and reliability are terms that are closely associated with electrical circuits since the transistor technology stepped into nanoscale regime of operation. Quantum mechanical phenomena and manufacturing limitations introduced process parameter variations and time-based degradations. These generated a significant challenge to both designers and electronic design automation (EDA) community in terms of modeling, simulation, and testing. Analog and mixed-signal circuits are particularly impacted by these challenges because satisfying multiple design specifications such as timing, noise, and power, constraints becomes significantly difficult in a much smaller feasible design space. In this talk I will introduce approaches that aim to deal with the multiple sides of the problem described.

The first part of the talk will focus on the modeling and simulation side. Neural network-based reduced-order models for the DC drain current, *Ids*, of n- and p-channel transistors have been generated in terms of six process parameters, terminal voltages, junction temperature, and device age. These models enable concurrent analysis of process variations and reliability degradations in analog and mixed-signal circuits. The impact of process mismatch with and without the aging effects of several analog building blocks are evaluated using the developed models. Recommendations regarding design for reliability are made based on the analysis outcomes.

The second part of the talk will concentrate on the testing side of the problem. Analog circuits embedded in large mixed-signal designs can fail due to unexpected process parameter excursions. To evaluate manufacturing tests in terms of their ability to detect such failures, parametric faults leading to circuit failures should be identified. Here, an iterative sampling method is proposed to identify these faults in large-scale analog circuits with a constrained simulation budget. Experiment results on two circuits from a serial IO interface demonstrate the effectiveness of the methodology. The proposed method identifies a significantly larger and diverse set of critical parametric faults compared to a Monte Carlo-based approach for identical computational budget, particularly for cases involving significant process variations.

Short Bio:

Mustafa Berke Yelten was born in Istanbul, Turkey, in 1982. He received the B.S. degree in electrical engineering from Bogazici University, Istanbul, Turkey in 2006 and the M.S. and Ph.D. degrees in electrical engineering from North Carolina State University, Raleigh, NC, USA in 2008 and 2011, respectively. Since October 2011, he has been with Intel Corporation, Hillsboro, OR, USA. In his Ph.D. dissertation, he focused on the computer-aided design (CAD) and mathematical modeling techniques for the variability and reliability analysis of analog circuits. His current research interests include the design,

testing, modeling and simulation of variability- and reliability-aware analog/RF, digital and mixed-signal integrated circuits.